Research and Analysis on Performance Improvement of Transmission Delay Caused by BTI Aging

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ABSTRACT

In the field of the transmission delay of input buffer, the problem of delay caused by BTI (Bias Temperature Instability) aging is very concerned about to researchers. With the addition of a new generation of process design, the research of BTI has become the most critical mechanism. This paper mainly discusses the important breakthrough obtained by establishing aging model and standard logic unit after accurate estimation and comprehensive analysis. A typical example in this paper is using LTSPICE software to simulate and design in 32 nm CMOS process. Through the simulation results, it can be concluded that the transmission delay of Schmitt flip-flops which is input buffer in this design is significantly improved. Although affected by BTI aging, the transmission delay of 11 cascaded CMOS inverters is increased by about 30% and the delay is reduced by above half compared to before. The need of increasing reliability is optimized by combining with ALI and AHI technology, which reduces the transmission delay by about 35%.

CCS CONCEPTS

• **Networks**; • **Network performance evaluation**; • **Network performance analysis**;

KEYWORDS

Input buffer, BTI Aging, Transmission delay, Isolation cells

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1 INTRODUCTION

At first, we used traditional 'Hot Carrier Injection' (HCI) to improve reliability, but with the development of MOSFETs, we added nitrided gate oxides, such as SiO2 [1]. Due to its own shortcomings, the influence of 'Bias Temperature Instability' (BTI) increases, which is also the focus of this paper how to reduce and optimize the transmission delay caused by BTI aging is the focus of this paper. At present, most of the research topics are about the improvement of stability and efficiency. Therefore, as a traditional gate oxide medium, SiO2 is far from meeting this demand.

Based on the above bottlenecks, scholars have studied FD-SOI as a candidate technology, which has the advantages of High-K(HK) value and metal gate [2]. The feasibility of this technology is verified by reliability measurement. Metal gate (MG) solves the shortcomings of traditional materials such as SiO2, thus HKMG MOSFET will be developed and put into use eventually.

With the improvement of technology and demand of users, the shortcomings of HK are exposed, especially the defects of charge. Therefore, the research on BTI has entered a rapid development. Some scholars have proposed a new technology for to detect recycled ICs via an on-chip, coarse-grained aging sensor, which can be applied to low-power circuits featuring power gating [3].

In addition to the needs of users, the recycling and reuse of electronic components are also the focus of the society and governments. Safety and reliability are the basis of electronic components [4].

This is also one of the reasons to research the performance electronic components of BTI aging . It can not only increase the service life of electronic systems, but also has important significance for environmental protection issues such as recycling. In the design of integrated system, there are several design points in the design of high-speed CMOS integrated circuit, such as full swing of voltage, switching speed and power distribution [5].For high-performance, low-power CMOS driver, CMOS Schmitt flip-flop is a good choice,

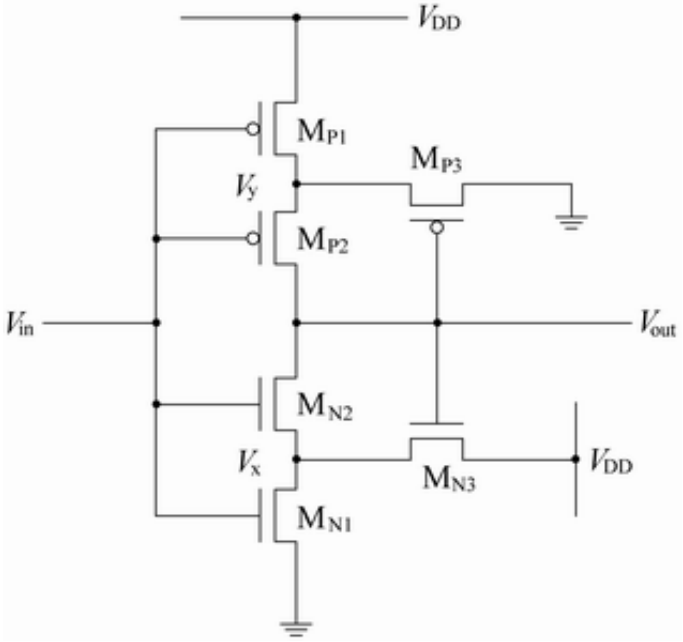

Figure 1: Schmitt Flip-Flop of Input Buffer.

as shown in Figure 1 [6], which is the research object of this paper. Taking this Schmitt flip-flop of input buffer as an example, the performance analysis of input buffer under the influence of BTI aging in 32nm CMOS process is researched.

The effects of BTI aging on electronic components have been researched for many years and the research papers are relatively mature. However, as time goes on, there has not been a lot of research and major breakthrough on the transmission delay of input buffer.Therefore, this is the reason for this paper to study.

The paper is divided into five sections. The first part introduces the background and current research status. The second part introduces the principle and process of the design approach in detail. In the third part, the influence of BTI aging on Schmitt input buffer is analyzed through the simulation results. The fourth part is optimized by ICMT technology, and the last part is the summary of this research.

2 BTI AGING MODEL AND SIMULATION APPROACH

The second part is the principle and model of design approach, which is the premise and foundation of simulation and optimization. In this section, the principle and detailed formula of BTI aging model are introduced. The simulation method will also be introduced in detail, and the flow chart will also be shown below.

2.1 BTI Aging Model

(1)Device aging further weakens the soft error sensitivity and SNM of low-power memory. Bias temperature instability (BTI) is considered to be the main parameter failure mechanism of some nano CMOS technologies. Its main function is to increase the threshold voltage (Vth) of MOS transistors [7]. In some technologies, in order to ensure high reliable data retention in low power memory, the negative effect of aging on memory reliability is considered when selecting the minimum voltage. However, this technique ignores the positive effect of BTI induced aging on the reduction of subthreshold current.

The unstable temperature polarization effect increases the threshold voltage of the MOS transistor.(stress phase) When the MOS transistor is biased (recovery phase), the degradation caused by BTI is recovered. The negative BTI (NBTI) observed in the INMOS transistor is generally consistent with the positive BTI (NBTI) observed in NMOS transistors [8]. The decentralized model designer's estimate response provides method parameters, operating conditions and time functions. The storage does not depend on the frequency of the input signal and does not depend on the total time stress [(1)] provides a simple analysis model that enables the designer to estimate the long-term voltage threshold. This is:

$$\Delta V_{th} = \chi K \sqrt{C_{ox}\left(V_{dd} - V_{th}\right)\alpha^{1/6} t^{/6}} \tag{1}$$

Obviously, the ΔV_{th} has three changes, the '∂ ' has to do with the signal probability and frequency of the transistor. In addition, 'K_{AC}' is a technology and supply voltage oriented constant.
The 't ' represents stress time (aging time) which uses seconds as the unit of measurement.The Cox parameter is the oxidation capacitance, t is the run time, and a is part of the run time, during which the transistor is under pressure. A = 0 if the transistor still fails (recovery phase) and a = 1 if it is still operating (stress phase). The x-coefficient can distinguish pBTI from NBTI [9].In this paper, we research the transmission delay of BTI aging under different DC power.

2.2 The Simulation Approach

According to BTI aging model, different Vth values are calculated in the simulation process. Due to the transmission delay caused by BTI aging over time, five time points are intercepted from 1 to 10 years to calculate the Vth value. It is the bias tempereture stability that belongs to the problems that affecting the CMOS process, so the severity of BTI aging needs to be paid attention to and improved. Simulation results show that BTI seriously limits the reliability design of memory, especially when the random process changes [10][11]. After simulation with LTspice software, the corresponding conclusions are obtained by collecting data. The simulation approach is to establish BTI aging model and calculate the value of Vth, to determine the corresponding value for simulation, using LTspice and SPICE netlist to get the results and analysis. Figure 2 shows a more detailed block diagram of the simulation approach structure.
The research center of this project focuses on analyzing the impact and improvement of the BTI ageing model in input buffer.Therefore, it is very important to choose an appropriate BTI aging model. This is the basis and premise of correct simulation results that this paper need. In this paper, 32 nm technology and DC reaction diffusion model constitute the BTI aging model. It should be noted that the power supply voltage almost does not affect the Vth value of the BTI aging model. Therefore, the power supply voltage and power range can be determined firstly referring to the standard of 32 nm

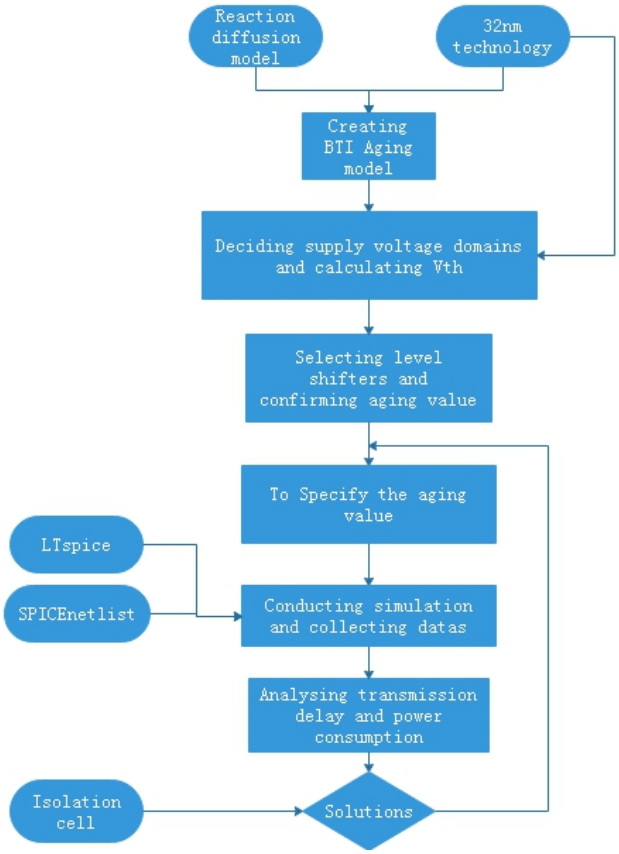

Figure 2: Simulation Design Process of the Project.

technology. When the aging value of Vth is determined, the level converter could also be selected.

The reason why the 32 nm HKMG technology has become the choice of BTI aging model in this paper is that in the field of semiconductor, whether in China or worldwide [12], the 32 nm HKMG technology is preferred by the professional technical support personnel, which is the future development trend and the result of many years of research.Thus, both the length with P-type MOSFETs and the thickness in N-type MOSFETs are 32nm.After BTI aging model is established and the parameters are selected, the cycle simulation process is started. According to the formula in 2.1, the aging value Vth is obtained by the relationship between Vdd and the voltage between the grid and the source. After the aging value Vth is determined, the software for simulating and receiving the data is called LT Spice, which sets the same temperature and aging time (in years). Transmission delay and average power consumption are the data needed been collected. Another software, SPICE, is used to create the library and operate correctly according to the user's manual [13]l. The purpose is to create MOSFET for better analysis of transmission delay and power consumption.

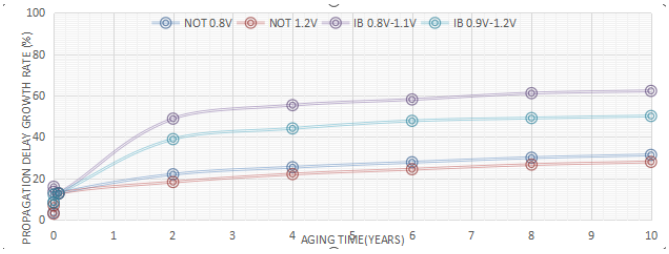

Figure 3: Comparison with the Propagation Delay Growth Rate between Input Buffer and 11- cascaded NOT Gate.

3 ANALYSIS THE TRANSMISSION DELAY OF BTI AGING

In the simulation process, five important time nodes are intercepted in the second, fourth, sixth, eighth and tenth year of the use process. The collected data of simulation is drawn into a line chart, which can more clearly and intuitively reflect the growth curve of transmission delay with years under different power supply voltages. The line diagram is shown in Figure 3. First of all, this intuitive curve clearly tells us that the performance of transmission delay is better than 0.8-1.1V when the voltage is at 0.9-1.2v. The transmission delay of 0.9-1.2v is smaller and much smaller for the same component and the same service time. The growth rates of these two curves are similar, but the values at 0.9-1.2v are much smaller. Under the supply voltage of 0.8-1.1V, the input buffer has experienced ten years of use and BTI aging, and the transmission delay has increased significantly by nearly 80%. Similarly, in the case of 0.9-1.2v, although the value is significantly smaller than 0.8-1.1V, the growth rate of transmission delay is close to 80%. However, when comparing IB 0.8-1.1V and NOT-chain 0.8V, we can see that the transmission delay of NOT-chain 0.8V increases slowly, almost only half. To cause the phenomenon has been increased of threshold voltage caused by BTI aging, especially under Schmitt flip flow of input buffer.

4 PROPOSED TECHNIQUE

4.1 Isolation Cell

In CMOS digital logic circuit, the design requirement is low power consumption, so the main factor of transmission delay of input buffer is that when the power supply of a circuit needs to be cut off, the output of the circuit will appear indefinite value. Therefore, in this phenomenon, it is necessary to add an isolation cell between the output of the circuit and its connected modules. When the power is turned off, the output network is fixed at a certain level. After the power is turned on, the output of the circuit is equal to the input, and the function of the circuit is not affected. In low power design, the most common isolation cells are NAND-style Isolation Cell and OR-style Isolation Cell.

First of all, as shown in Figure 4, isolation cell can be realized by using logic gate, AND gate can realize that output is 0 when power is turned off, and 1 when power is turned off by using OR gate. ISOLN and ISOL are switch control signals respectively [14].

The NAND of isolation cell functions to force output signal to the ground, which named from Active Low Isolation (ALI).Through ALI

Figure 4: Isolation Cell Composed of Logic Gates.

technology, also named NAND-style isolation cell, the transmission delay caused by BTI aging can be significantly improved. But it can not directly solve the problem of delay, which is the reaction of high voltage. The floating signal still exists and is continuously input into the ALI circuit. In addition, SPICE network will also cause a lot of impact, because BTI aging not only causes transmission delay, but also affects the transistor of isolation unit. Therefore, the only use of ALI technology of NAND-style isolation cell can not completely solve the problem, still need further improvement

Figure 5 is the principle of NAND-style Isolation Cell, of which composed by an inverter and NAND gate.When the ISOLN port is assigned VSS,the OUT port also remain at VDDH. Since the input signal is isolated from the entire gate, this can happen regardless of the input port. Preventing the output signal of input floating signal is the main function of isolation unit.

Apart from the common NAND isolation unit, another isolation unit technology is or isolation unit.Different from NAND-style, when we set ISOL signal to high level, it has a feature of keeping the output signal at the original high level value. This is the opposite of ISOLN in ALI technology, which is usually called Active High Isolation (AHI). Through AHI technology, also named OR-style isolation cell, the transmission delay caused by BTI aging can be significantly improved slowly. But it can not directly solve the problem of delay, which is the increased propotion of high voltage. Although the delay increases slowly, another defect has emerged, which will cause the floating signal to transmit to the next power domain. Embedded AHI technology, resulting in high levels, will make the conductivity of transistors decline sharply with the growth of years. Therefore, using AHI technology alone will bring more threats and challenges.

Figure 6 is the principle of OR-style Isolation Cell, of which composed by an inverter and NOR gate. The operational principle is similar with the ALI technique.However, in AHI technique, ISOL stands for input logic '1'. Meanwhile, when the floating signal is transmited to the input port, the output port level will also be clamped to VDDH.

4.2 Proposed BTI Aging Mitigating Technique

This paper to discuss the advantages and shortcomings of type NAND and type OR separation units.Their corresponding technologies are ALI and AHI. Through simulation and analysis, it can be concluded that ALI and AHI technologies are complementary to each other to some extent. This idea is to combine the advantages of this two technologies to make up for each other's shortcomings, so as to improve the transmission delay performance caused by BTI aging in Schmitt flip-flop of input buffer.Figure 7 is the principle of combine with the NAND-style and OR-style separation cells. Combining the advantages of this two isolation cells, that is, the input of ALI is directly connected to the output of the level shifter. This operation allows the signal to pass through ALI and AHI smoothly.

In order to verify this assumption, and to check whether the transmission delay caused by BTI aging problem has been improved, LTSpice software is still used to simulate under two different power

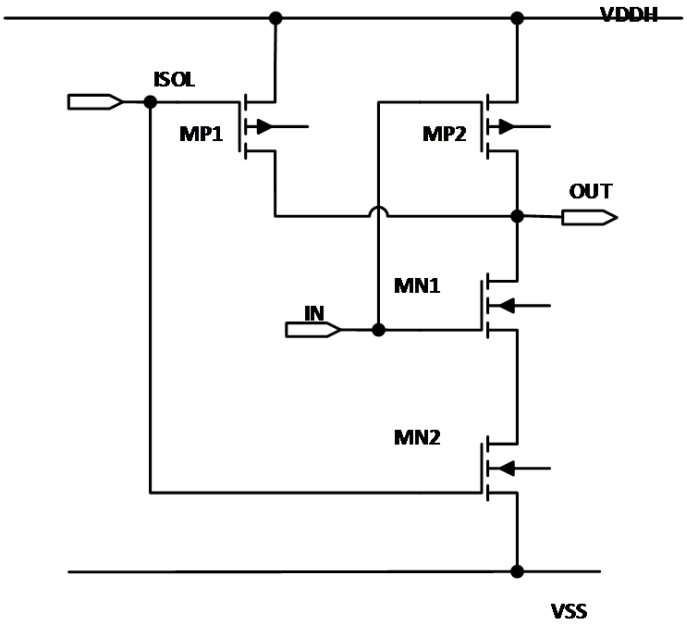

Figure 5: Schematic of AND-style Isolation Cell.

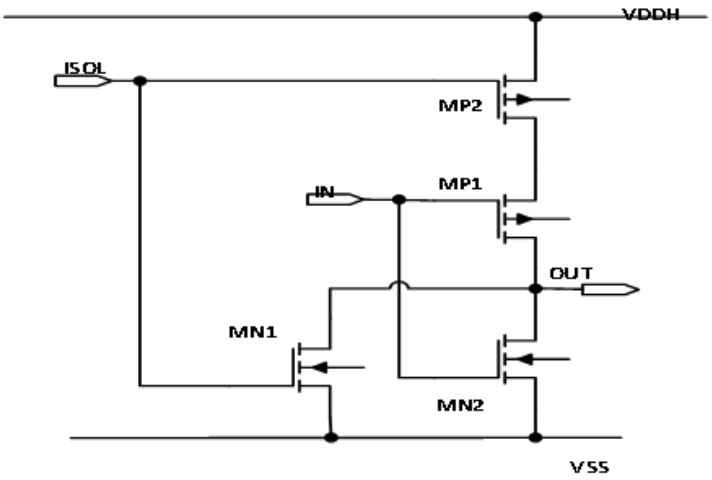

Figure 6: Schematic of OR-style Isolation Cell.

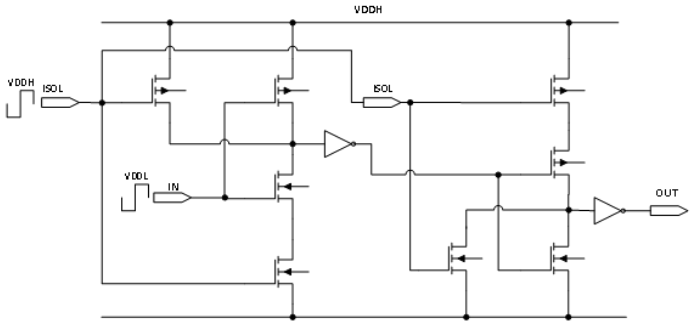

Figure 7: Schematic of Combine with the NAND-style and OR-style Isolation Cells.

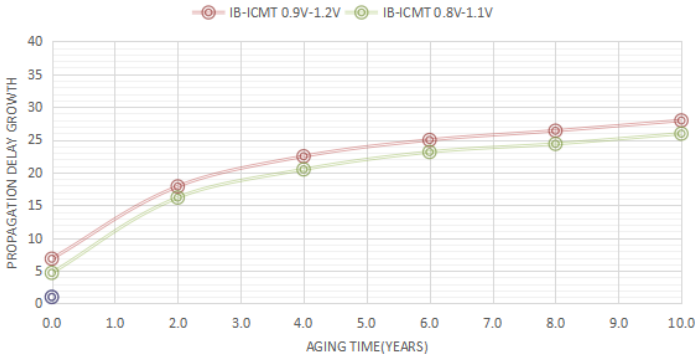

Figure 8: BTI-aware Propagation Delay of Input Buffer with ICMT.

supply voltages, and the parameters are the same as those in the third sections. The simulation results show that this method can alleviate the transmission delay caused by BTI aging, and compared with the single simulation approach, the simulation results combining ALI and AHI technology can significantly improve the mitigation effect, as shown in figure 8. Compared with figure 3, the transmission delay caused by BTI aging is optimized.

Transmission delay of CMOS 11-cascaded inverters is increased by about 30% and the delay is reduced by above half compared to before. The need of increasing reliability is optimized by combining

with ALI and AHI technology, which reduces the transmission delay by about 35% in 0.8-1.1V.

5 CONCLUSIONS

This paper proves that two kinds of isolation cells can be combined to form a new technology. And for the input buffer in the integrated circuit, after BTI aging, it can also play a positive role in the transmission delay. The new technology combines NAND-style and OR-style isolation cells, which can not only greatly alleviate the impact of BTI aging, but also alleviate the high level. Through the embodiment of the simulation results and the analysis of the results of two simulations, a conclusion is obtained that the fusion technology solves the bottleneck of BTI aging problem, and the mitigation effect is remarkable. But at the same time, through the simulation results, this paper also draws a conclusion that although the delay caused by BTI aging has been alleviated, the transmission delay still exists, which can not be ignored. Therefore, when the circuit designer designs the integrated circuit system, he must consider the time period, otherwise the reliability of the system will get negative feedback. The error still exists, and the research still needs to continue.

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REFERENCES

[1] C. Schlünder *et al.* (2012). HCI vs. BTI? - Neither one's out. 2012 IEEE International Reliability Physics Symposium (IRPS), Anaheim, CA, 2012, pp. 2F.4.1-2F.4.6, doi: 10.1109/IRPS.2012.6241797.

[2] M. Agarwal, V. Balakrishnan, A. Bhuyan, K. Kim, B. C. Paul, W. Wang, B. Yang, Y Cao, and S. Mitra (2008). Optimized circuit failure prediction for aging: Practicality and promise, in Proc. of IEEE International Test Conference (ITC), pp. 1-10.

[3] A. Bardine, M. Comparetti, P. Foglia, and C. A. Prete (2014). Evaluation of leakage reduction alternatives for deep submicron dynamic nonuniform cache architecture caches. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 22, no. 1, pp. 185-190.

[4] J. Cai, B. Halak and D. Rossi (2016). Analysis of BTI aging of level shifters, 2016 IEEE 22nd International Symposium on On-Line Testing and Robust System Design (IOLTS), Sant Feliu de Guixols, pp. 17-18, doi: 10.1109/IOLTS.2016.7604662.

[5] V. Tenentes, D. Rossi, S. Yang, S. Khursheed, B. M. Al-Hashimi and S. R. Gunn (2017). Coarse-Grained Online Monitoring of BTI Aging by Reusing Power-Gating Infrastructure, in IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 25, no. 4, pp. 1397-1407, April 2017, doi: 10.1109/TVLSI.2016.2626218.

[6] H. David, C. Fallin, E. Gorbatov, U. R. Hanebutte, and O. Mutlu (2011). Memory power management via dynamic voltage/frequency scaling, in Proc. of the 8th ACM international conference on Autonomic computing, pp. 31-40.

[7] I. Lin, Y. Cho and Y. Yang (2015). Aging-Aware Reliable Multiplier Design With Adaptive Hold Logic, in IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 23, no. 3, pp. 544-556, March 2015.

[8] Z. H. Gan *et al.* (2006). Models of Source/Drain Bias on Negative Bias Temperature Instabilit. 2006 8th International Conference on Solid-State and Integrated Circuit Technology Proceedings, Shanghai, 2006, pp. 1119-1121, doi: 10.1109/ICSICT.2006.306699.

[9] D. Rossi, V. Tenentes, S. Khursheed and B. M. Al-Hashimi (2015). BTI and leakage aware dynamic voltage scaling for reliable low power cache memories. 2015 IEEE 21st International On-Line Testing Symposium (IOLTS), Halkidiki, pp. 194-199, doi: 10.1109/IOLTS.2015.7229858.

[10] N. S. Kim, K. Flautner, D. Blaauw, and T. Mudge (2004). Circuit and microarchitectural techniques for reducing cache leakage power. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 12, no. 2, pp. 167-184.

[11] S. P. Park, K. Kang and K. Roy (2009). Reliability Implications of Bias-Temperature Instability in Digital ICs, in IEEE Design & Test of Computers, vol. 26, no. 6, pp. 8-17, Nov.-Dec. 2009.

[12] D. Varghese, D. Saha, S. Mahapatra, K. Ahmed, F. Nouri and M. Alam (2005). On the dispersive versus arrhenius temperature activation of nbti time evolution in plasma nitrided gate oxides: measurements, theory, and implications. IEEE InternationalElectron Devices Meeting, 2005. IEDM Technical Digest., Washington, DC, pp. 684-687, doi: 10.1109/IEDM.2005.1609444.

[13] A. Nourivand, A. J. Al-Khalili, and Y. Savaria (2012). Postsilicon tuning of standby supply voltage in srams to reduce yield losses due to parametric data-retention failures," IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 20, no. 1, pp. 29-41.

[14] K. Michael, F. David, A. Robert, *et al.* (2007). Low power methodology manual: for system-on-chip design. New York, USA: Springer Publishing Company, LLC.